In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

1   1.   (Currently Amended) An apparatus, comprising:

2   an integrated circuit including:

3   a first processor with a first dedicated cache;

4   a second processor with a second dedicated cache; and

5   control logic coupled to the first and second dedicated caches to <u>receive</u>

6   ~~transfer~~ first data from the first dedicated cache <u>and</u> to <u>transfer</u> the

7   <u>first data to the</u> second dedicated cache entirely within the integrated

8   circuit.

1   2.   (Original)   The apparatus of claim 1, wherein:

2   the control logic is to transfer the first data if the first data is a cache line in the first

3   dedicated cache and not in the second dedicated cache.

1   3.   (Original)   The apparatus of claim 1, wherein:

2   the control logic is to transfer the first data if the first data is a modified version of

3   a particular cache line and the second dedicated cache contains an

4   unmodified version of the particular cache line.

1   4.   (Original)   The apparatus of claim 1, further comprising:

2   a coherency unit to perform snoop operations on the first and second dedicated

3   caches.

1   5.   (Original)   The apparatus of claim 1, wherein:

2   the control logic is further to transfer second data from the second dedicated cache

3   to the first dedicated cache entirely within the integrated circuit.

1 6.   (Original)   The apparatus of claim 1, wherein the integrated circuit further

2 includes:

3   a shared cache coupled to the control logic and to the second dedicated cache to

4   provide the first data to the second dedicated cache;

5   wherein the control logic includes a write buffer to receive the first data from the

6   first dedicated cache and to provide the first data to the shared cache.

1 7.   (Original)   The apparatus of claim 1, wherein the integrated circuit further

2 includes:

3   a shared cache coupled to the control logic, to the first dedicated cache, and to the

4   second dedicated cache;

5   wherein the control logic is further to transfer second data from the second

6   dedicated cache to the first dedicated cache;

7   wherein the control logic includes a first write buffer to receive the first data from

8   the first dedicated cache and to provide the first data to the shared cache,

9   and further includes a second write buffer to receive the second data from

10   the second dedicated cache and provide the second data to the shared cache;

11   wherein the shared cache is to provide the first data to the second dedicated cache

12   and to provide the second data to the first dedicated cache.

1 8.   (Original)   The apparatus of claim 1, wherein:

2   the control logic includes a fill buffer coupled to first and second dedicated caches

3   to receive the first data from the first dedicated cache and to provide the

4   first data to the second dedicated cache.

1   9.   (Original)   The apparatus of claim 1, wherein:

2   the control logic includes a first fill buffer coupled to the first and second dedicated

3   caches to receive the first data from the first dedicated cache and to provide

4   the first data to the second dedicated cache; and

5   the control logic includes a second fill buffer coupled to the first and second

6   dedicated caches to receive second data from the second dedicated cache

7   and to provide the second data to the first dedicated cache

1   10.   (Original)   The apparatus of claim 1, wherein the control logic includes:

2   a multiplexer coupled to the first and second caches to receive the first data from

3   the first dedicated cache and to provide the first data to the second dedicated

4   cache.

1   11.   (Original)   The apparatus of claim 1, wherein the control logic includes:

2   a first multiplexer coupled to the first and second caches to receive the first data

3   from the first dedicated cache and to provide the first data to the second

4   dedicated cache; and

5   a second multiplexer coupled to the first and second caches to receive second data

6   from the second dedicated cache and to provide the second data to the first

7   dedicated cache.

1   12.   (Original)   A method, comprising:

2   transferring first data from a first dedicated cache of a chip multi-processor to

3   control logic in the chip multi-processor, entirely within the chip multi-

4   processor; and

5   subsequently transferring the first data from the control logic to a second dedicated

6   cache of the chip multi-processor, entirely within the chip multi-processor.

1   13.   (Original)   The method of claim 12, further comprising:

2   transferring second data from the second dedicated cache to the control logic,

3   entirely within the chip multi-processor; and

4   subsequently transferring the second data from the control logic to the first

5   dedicated cache, entirely within the chip multi-processor.

1   14.   (Original)   The method of claim 12, wherein:

2   the transferring the first data from the first dedicated cache includes transferring the

3   first data from the first dedicated cache to a write buffer;

4   the transferring the first data from the control logic includes transferring the first

5   data from the write buffer to a shared cache.

1   15.   (Original)   The method of claim 14, wherein:

2   the transferring the first data from the control logic further includes transferring the

3   first data from the shared cache to the second dedicated cache.

1   16.   (Original)   The method of claim 12, wherein:

2   the transferring the first data from the first dedicated cache includes transferring the

3   first data from the first dedicated cache to a fill buffer;

4   the transferring the first data from the control logic includes transferring the first

5   data from the fill buffer to the second dedicated cache.

1   17.   (Original)   The method of claim 12, wherein:

2   the transferring the first data from the first dedicated cache includes transferring the

3   first data from the first dedicated cache to a multiplexer; and

4   the transferring the first data from the control logic includes transferring the first

5   data from the multiplexer to the second dedicated cache.

1   18.   (Currently Amended) A system, comprising:

2   a main memory,

3   a chip multiprocessor coupled to the main memory and including:

4   a first processor with a first dedicated cache;

5   a second processor with a second dedicated cache; and

6   control logic coupled to the first and second dedicated caches to <u>receive</u>

7   ~~transfer~~ first data from the first dedicated cache <u>and</u> to <u>transfer</u> the

8   <u>first data to the</u> second dedicated cache entirely within the integrated

9   circuit.

1   19.   (Original)   The system of claim 18, wherein:

2   the control logic is further to transfer second data from the second dedicated

3   cache to the first dedicated cache entirely within the chip

4   multiprocessor.

1   20.   (Original)   The system of claim 18, wherein the chip multiprocessor further

2 includes:

3   a shared cache coupled to the control logic and to the second dedicated cache to

4   provide the first data to the second dedicated cache;

5   wherein the control logic includes a write buffer to receive the first data from the

6   first dedicated cache and to provide the first data to the shared cache.

1   21.   (Original)   The system of claim 18, wherein:

2   the control logic includes a fill buffer coupled to first and second dedicated caches

3   to receive the first data from the first dedicated cache and to provide the

4   first data to the second dedicated cache.

1   22.   (Original)   The system of claim 18, wherein the control logic includes:

2   a multiplexer coupled to the first and second dedicated caches to receive the first

3   data from the first dedicated cache and to provide the first data to the second

4   dedicated cache.

1   23.   (Original)   A machine-readable medium that provides instructions, which when

2   executed by a set of one or more processors, cause said set of processors to perform

3   operations comprising:

4   transferring data from a first dedicated cache in an integrated circuit to control logic

5   in the integrated circuit, entirely within the integrated circuit; and

6   subsequently transferring the data from the control logic to a second dedicated

7   cache of the integrated circuit, entirely within the integrated circuit.

1   24.   (Original)   The medium of claim 23, wherein:

2   the transferring the data from the first dedicated cache includes transferring the data

3   from the first dedicated cache to a write buffer; and

4   the transferring the data from the control logic includes transferring the data from

5   the write buffer to a shared cache and subsequently transferring the data

6   from the shared cache to the second dedicated cache.

1   25.   (Original)   The medium of claim 23, wherein:

2   the transferring the data from the first dedicated cache includes transferring the data

3   from the first dedicated cache to a fill buffer; and

4   the transferring the data from the control logic includes transferring the data from

5   the fill buffer to the second dedicated cache.

1   26.   (Original)   The medium of claim 23, wherein:

2   the transferring the data from the first dedicated cache includes transferring the data

3   from the first dedicated cache to a multiplexer; and

4   the transferring the data from the control logic includes transferring the data from

5   the multiplexer to the second dedicated cache.